L Number	Hits	Search Text	DB	Time stamp
7	0	((processor or multiprocessor or microprocessor) near3	USPAT;	2003/10/18 15:16
		(contain\$3 or hold\$3 or includ\$3 or hav\$3 or has)) near3	US-PGPUB;	
		((MOS and transistor) and gate)	EPO; JPO;	•
			DERWENT;	
		<u>.</u>	IBM_TDB	
8	205	((processor or multiprocessor or microprocessor or	USPAT;	2003/10/18 15:21
		semiconductor or chip or (integrated adj circuit)) near3	US-PGPUB;	
	·	(contain\$3 or hold\$3 or includ\$3 or hav\$3 or has)) near3	EPO; JPO;	
		(MOS and transistor and gate)	DERWENT;	
		//	IBM_TDB USPAT;	2003/10/18 15:18
9	0	((processor or multiprocessor or microprocessor or semiconductor or chip or (integrated adj circuit)) near3	US-PGPUB;	2003/10/16 15.16
		(contain\$3 or hold\$3 or includ\$3 or hav\$3 or has)) near3	EPO; JPO;	
		(p-MOS and n-MOS and transistor and gate)	DERWENT;	1
		(p-WOS and 11-WOS and transistor and gate)	IBM_TDB	
10	1	((processor or multiprocessor or microprocessor or	USPAT;	2003/10/18 15:20
10	•	semiconductor or chip or (integrated adj circuit)) near3	US-PGPUB;	2003/10/10 13:20
		(contain\$3 or hold\$3 or includ\$3 or hav\$3 or has)) near3	EPO; JPO;	
		(MOS and MOS and transistor and gate) and 716/\$.ccls.	DERWENT;	
		(Woo and Woo and Canolists and gate) and 7 to 4.000	IBM_TDB	
11	1	((processor or multiprocessor or microprocessor or	USPAT;	2003/10/18 15:20
' '		semiconductor or chip or (integrated adj circuit) or IC) near3	US-PGPUB;	
		(contain\$3 or hold\$3 or includ\$3 or hav\$3 or has)) near3	EPO; JPO;	
		(MOS and MOS and transistor and gate) and 716/\$.ccls.	DERWENT;	;
			IBM_TDB	
12	210	((processor or multiprocessor or microprocessor or	USPAT;	2003/10/18 15:22
		semiconductor or chip or (integrated adj circuit) or IC) near3	US-PGPUB;	
		(contain\$3 or hold\$3 or includ\$3 or hav\$3 or has)) near3	EPO; JPO;	
		(MOS and transistor and gate)	DERWENT;	
			IBM_TDB	
13	29	((processor or multiprocessor or microprocessor or	USPAT;	2003/10/18 16:20
		semiconductor or chip or (integrated adj circuit) or IC) near3	US-PGPUB;	
		(contain\$3 or hold\$3 or includ\$3 or hav\$3 or has)) near3	EPO; JPO;	
		(MOS and transistor and gate) and symmetric\$3	DERWENT; IBM_TDB	
14	0	(MOS adj transostor) same (width and length)	USPAT;	2003/10/18 16:21
14		(who o adjulansostor) same (whath and length)	US-PGPUB;	2000/10/10 10.21
			EPO; JPO;	
			DERWENT;	
			IBM TDB	
15	2428	(MOS adj transistor) same (width and length)	USPAT;	2003/10/18 16:21
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
16	222	((MOS adj transistor) same (width and length)) and processor	USPAT;	2003/10/18 16:21
			US-PGPUB;	
			EPO; JPO;	
]			DERWENT;	
17	_	(MOS adi transister) same (width and largeth)) same	IBM_TDB	2002/40/49 40:00
''	3	((MOS adj transistor) same (width and length)) same	USPAT; US-PGPUB;	2003/10/18 16:28
		processor	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
28	63	((MOS adj transistor) same (width and length)) same (orient\$4	USPAT;	2003/10/18 16:31
		or plac\$3 or orientation)	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
29	8	(((MOS adj transistor) same (width and length)) same	USPAT;	2003/10/18 16:31
		(orient\$4 or plac\$3 or orientation)) and symmetric\$3	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	

2 5787310,pn. 2 5787310,pn. 2 5787310,pn. 2 5787310,pn. 2 10 ((on adj chip adj processor) same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 2 10 ((on adj chip near3 processor) same layout) and ((multiple or plurality) near3 processor) same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 3 10 (((on adj chip) near3 processor) same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 3 10 (((on adj chip) near3 processor) same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 4 (((on adj chip) near3 processor) and (ayout near3 (multuple or plurality) near3 processor) and (((on adj chip) near3 processor) and (ayout near3 (multuple or plurality) near3 processor) (((on adj chip) near3 multiprocessor) and (ayout near3 (multuple or plurality) near3 processor) (((on adj chip) near3 multiprocessor) and (((on adj chip) near3 processor) (((on adj chip) near3 multiprocessor) and ((((on adj chip) near3 multiprocessor) and ((((on adj chip) near3 multiprocessor) (((on adj chip) near3 multiprocessor) and ((((on adj chip) near3 multiprocessor) (((((on adj chip) near3 multiprocessor) (((((in adj chip) near3 multiprocessor) (((((in adj chip) near3 near) ((((((in adj chip) near3 near) ((((((((((((((((((((((((((((((((((((100
EPO, JPO; DERWENT; IBM, TDB USPAT; US-PG-PUB; EPO, JPO; DERWENT; IB	-	2	5787310.pn.	USPAT;	2003/10/15 14:43
- 0 ((on adj chip adj processor) same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 - 0 ((on adj chip near3 processor) same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) same layout) and ((multiple or plurality) near3 processor) - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 ((((on adj chip) near3 processor) and symmetric\$3 - 0 ((((on adj chip) near3 processor) and symmetric\$3 - 0 ((((on adj chip) near3 processor) and symmetric\$3 - 0 (((((on adj chip) near3 processor) and symmetric\$3 - 0 (((((((((((((((((((((((((((((((((((
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- 0 ((on adj chip near3 processor) same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 (((on adj chip) near3 processor) and symmetric\$3 - 0 ((((n) adj chip) near3 processor) and symmetric\$3 - 0 ((((n) adj chip) near3 processor) and symmetric\$3 - 0 ((((n) adj chip) near3 processor) and symmetric\$3 - 0 ((((n) adj chip) near3 processor) and symmetric\$3 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$3 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$3 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$3 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$3 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$3 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 (((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 ((((n) adj chip) near3 multiprocessor) and symmetric\$4 - 0 (((((n) adj chip) near3 multiproce	-	0	((on adj chip adj processor) same layout) and ((multiple or		2003/10/15 14:46
Comparison of the plane of th			plurality) near3 processor) and symmetric\$3		
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Discription		_			
-	-	0			2003/10/15 14:46
-			plurality) near3 processor) and symmetric\$3		
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Discription		0	(((an adjahin) near? processor) same layout) and ((multiple or		2002/10/15 14:46
Project Proj	-	0			2003/10/13 14.40
DERWENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB USP			plurality) hears processor) and symmetricas		
BM TDB Complain near3 multiprocessor) and (layout near3 (multuple adj processor)) BM TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT; US-PGPUB;					
Chip same layout) and ((multiple or plurality) near3 processor) USPAT;					
adj processor)) - 30 (chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 - 0 (chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 and ((inear adj axis)) - 0 (multiprocessor same chip) with ((ayout and symmetric\$3)) - 1174 (multiprocessor same chip) with ((ayout and symmetric\$3)) - 1174 (multiprocessor same chip) - 1174 (multiprocessor same chip) and layout and symmetric\$4 - 1174 (multiprocessor same chip) and (((ayout or architecture) near3 symmetric\$4) - 1174 (multiprocessor same chip) and ((((ayout or architecture) near3 symmetric\$4) - 1174 (multiprocessor same chip) and ((((ayout or architecture) near3 symmetric\$4)) - 1175 ((((a) Shar\$3 same center same symmetric\$4) same ((((a) Shar\$3 same center same symmetric\$4)) - 1175 (((((a) Shar\$3 same center same symmetric\$4))) - 1176 (((((((a) Shar\$3 same center same symmetric\$4)))) - (((((((((((((((((((((((((((((((((_		(floornian near3 multiprocessor) and (layout near3 (multiple		2003/10/15 14:51
- 70 (chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3	-				2000/10/10 14:01
- 24 (multiprocessor same chip) and (layout and symmetric\$4 - 24 (multiprocessor same chip) and (layout and symmetric\$4) - 2 (shar\$3 same center same symmetric\$4) - 2 (shar\$3 same center same symmetric\$4) - 3 (multiprocessor same chip) and (layout and symmetric\$4 and (layout or architecture) near3 symmetric\$4) - 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) - 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) - 5 (chip same layout) and ((multiple or plurality) near3 processor) 10 (multiprocessor) 10 (multiprocessor) 10 (multiprocessor) 10 (multiprocessor same chip) 10 (multiprocessor same			auj processoriji		
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- (chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 - 0 (chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 and (linear adj axis) - 0 (chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 and (linear adj axis) - 0 (multiprocessor same chip) with (layout and symmetric\$3) - 1174 (multiprocessor same chip) with (layout and symmetric\$4) - 1174 (multiprocessor same chip) and layout and symmetric\$4 - 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) - 25 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) - 14 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) - 15 (chip same layout) and ((multiple or plurality) near3 processor) USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; D					
and symmetric\$3 - 0 (chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 and (linear adj axis) - 0 (multiprocessor same chip) with (layout and symmetric\$3) - 1174 (multiprocessor same chip) with (layout and symmetric\$4) - 30 (multiprocessor same chip) and layout and symmetric\$4 - 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) - 22 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) - 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) - 14 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) - 15	_	70	(chin same layout) and ((multiple or plurality) near3 processor)	_	2003/10/17 11:12
- 0 (chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 and (linear adj axis) - 0 (multiprocessor same chip) with (layout and symmetric\$3) - 1174 (multiprocessor same chip) - 1175 (multiprocessor same chip) - 1176 (multiprocessor same chip) and layout and symmetric\$4 - 1177 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) - 1176 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) - 1176 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) - 1176 (cPU near3 (architecture or layout)) - 1177 (multiprocessor same chip) and layout and symmetric\$4 and (cPU near3 (architecture or layout))					2000/10/17 11:12
- 0 (chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 and (linear adj axis) - 0 (multiprocessor same chip) with (layout and symmetric\$3) - 1174 (multiprocessor same chip) with (layout and symmetric\$3) - 30 (multiprocessor same chip) and layout and symmetric\$4 - 30 (multiprocessor same chip) and (layout or architecture) near3 symmetric\$4) - 24 (multiprocessor same chip) and (layout or architecture) near3 (architecture or layout)) - 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) - 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) - 2003/10/16 07:56 2003/1			and dyniniothops		
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EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB US-PGPUB; EPO; JPO; DERWENT; IBM_T					
- 0 (multiprocessor same chip) with (layout and symmetric\$3) DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; ISM_TDB USPAT; US-PGPUB; EPO; JPO; DERWE					
- 1174 (multiprocessor same chip) with (layout and symmetric\$3) USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWE					
US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; ISM_TDB USPAT; US-PGPUB; EPO; JPO;					
- 1174 (multiprocessor same chip) - 30 (multiprocessor same chip) and layout and symmetric\$4 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; ISM_TDB USPAT; US-PGPUB;	-	0	(multiprocessor same chip) with (layout and symmetric\$3)	USPAT;	2003/10/16 07:56
- 1174 (multiprocessor same chip) (multiprocessor same chip) and layout and symmetric\$4 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO;				US-PGPUB;	
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- 1174 (multiprocessor same chip) (multiprocessor same chip) and layout and symmetric\$4 (multiprocessor same chip) and layout and symmetric\$4 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout))					
- 24 (multiprocessor same chip) and (layout or architecture) near3 symmetric\$4) - 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) - 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) - 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) - 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB					
- 30 (multiprocessor same chip) and layout and symmetric\$4 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; ISPO; JPO;	-	1174	(multiprocessor same chip)		2003/10/16 07:56
- 24 (multiprocessor same chip) and layout and symmetric\$4 USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; USPAT; USPAT; USPAT; USPAPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; USPAT; USPAT; USPAT; USPAPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; USPAT; USPAT; USPAT; USPAPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; USPAT; USPAPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; USPAPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAT; USPAPUB; EPO; JPO; DERWENT; USPAT; USPAPUB; EPO; JPO; DERWENT; USPAT;					;
- 30 (multiprocessor same chip) and layout and symmetric\$4 US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; ISPGPUB; EPO; JPO; DER					
- 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 2 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 2003/10/16 12:08 2003/10/16 09:37 2003/10/16 09:37 2003/10/16 09:40 2003/10/16 12:41 2003/10/16 12:41					
- 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) - 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) - 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB US-PGPUB; EPO; JPO; DERWENT; IBM_TDB US-PGPUB; EPO; JPO; DERWENT; IBM_TDB US-PGPUB; EPO; JPO; DERWENT;			Consulting and a second of the Consulting and the c		2002/40/40 40 22
- 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 2 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 5 (BPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT;	-	30	(multiprocessor same cnip) and layout and symmetric\$4		2003/10/16 12:08
- 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 5 DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT;					
- 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) BM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT;					
- 24 (multiprocessor same chip) and ((layout or architecture) near3 symmetric\$4) 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 2003/10/16 09:37 2003/10/16 09:37 2003/10/16 09:37 2003/10/16 09:40 2003/10/16 12:41 2003/10/16 12:41					
symmetric\$4) 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 5 US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IS-PGPUB; EPO; JPO; DERW		24	(multiprocessor same chip) and ((lovout or architecture) near?		2003/10/16 00:27
- 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) EPO; JPO; DERWENT; IBM_TDB US-PGPUB; EPO; JPO; DERWENT; IBM_TDB US-PAT; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT;	1	24			2003/10/10 08.3/
- 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 5 DERWENT; IBM_TDB US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT;			- супппецто рт)		:
- 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 5 (shar\$3 same center same symmetric\$4) same (chip near3 US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT;		}			
- 2 (shar\$3 same center same symmetric\$4) same (chip near3 (architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) 4 (shar\$3 same center same symmetric\$4) same (chip near3 USPAT; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT;					
(architecture or layout)) 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; DERWENT; DERWENT; DERWENT;	-	2	(shar\$3 same center same symmetric\$4) same (chin pear3		2003/10/16 09:40
- 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT;		_			2300, 10, 10, 00, 40
- 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout)) (CPU near3 (architecture or layout)) DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT;			(a. a		
- 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout))					
- 4 (multiprocessor same chip) and layout and symmetric\$4 and (CPU near3 (architecture or layout))					
(CPU near3 (architecture or layout)) US-PGPUB; EPO; JPO; DERWENT;	-	4	(multiprocessor same chip) and layout and symmetric\$4 and		2003/10/16 12:41
EPO; JPO; DERWENT;					
DERWENT;			• "		,
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				IBM_TDB	

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-	15	multiprocessor and layout and symmetric\$4 and (CPU near3 (architecture or layout))	USPAT; US-PGPUB; EPO; JPO;	2003/10/16 12:44
			DERWENT;	
	15	multiprocessor and layout and symmetric\$4 and (CDLL poor3	IBM_TDB USPAT;	2003/10/16 12:44
-	'5	multiprocessor and layout and symmetric\$4 and (CPU near3 (architecture or layout)) and shar\$3	US-PGPUB;	2003/10/10 12.44
			EPO; JPO;	
			DERWENT;	
		15 A and (ODI)	IBM_TDB	00004040404047
-	14	multiprocessor and layout and symmetric\$4 and (CPU near3 (architecture or layout)) and shar\$3 and (center or central)	USPAT; US-PGPUB;	2003/10/16 12:47
		(aromostaro or rayouty) and charpo and (contor or contrary	EPO; JPO;	
			DERWENT;	
		11	IBM_TDB	0000404040
-	20	multiprocessor and layout and (symmetric\$4 or mirror) and (CPU near3 (architecture or layout)) and shar\$3 and (center or	USPAT; US-PGPUB;	2003/10/16 13:38
		central)	EPO; JPO;	
		,	DERWENT:	
			IBM_TDB	
-	20	multiprocessor and layout and (symmetric\$4 or mirror) and (CPU near3 (architecture or layout)) and (shar\$3 near3	USPAT; US-PGPUB;	2003/10/17 11:10
		component or element or unit) and (snars hears	EPO; JPO;	
		(37.10)	DERWENT;	
			IBM_TDB	
	6	multiprocessor and layout and (symmetric\$4 or mirror) and (CPU near3 (architecture or layout)) and (shar\$3 near3	USPAT; US-PGPUB;	2003/10/16 13:39
		(component or element or unit)) and (center or central)	EPO; JPO;	t .
		(companies of content of content (content of content of	DERWENT;	
	_		IBM_TDB	
-	2	6516442.pn.	USPAT;	2003/10/16 14:22
			US-PGPUB; EPO; JPO;	•
			DERWENT;	
			IBM_TDB	
-	4	multiprocessor and layout and (symmetric\$4 or mirror) and (CPU near3 (architecture or layout)) and (shar\$3 near3	USPAT; US-PGPUB;	2003/10/17 11:10
		component or element or unit) and (center or central) and	EPO; JPO;	:
		PLL	DERWENT;	
	44	(although board (although board (although board board (although board bo	IBM_TDB	
-	11	(chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 and PLL	USPAT; US-PGPUB;	2003/10/17 12:05
		and symmetricus and FEE	EPO; JPO;	
			DERWENT;	
		(skip come levent) and (/swittints as alway) \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	IBM_TDB	2002/42/47 42 42
-	6	(chip same layout) and ((multiple or plurality) near3 processor) and symmetric\$3 and PLL and recovery	USPAT; US-PGPUB;	2003/10/17 12:19
		and symmotrops and receivery	EPO; JPO;	
			DERWENT;	:
		5007500 pp	IBM_TDB	2002/40/47 40:00
-	2	5987590.pn.	USPAT; US-PGPUB;	2003/10/17 12:22
			EPO; JPO;	
			DERWENT;	
	244	processor same (PLL and eachs)	IBM_TDB	2002/40/47 42:02
-	244	processor same (PLL and cache)	USPAT; US-PGPUB;	2003/10/17 12:23
			EPO; JPO;	
			DERWENT;	:
_	1	(processor same (PLL) and cache)) and this and (numeration?)	IBM_TDB	2002/40/47 42:25
-	'	(processor same (PLL and cache)) and chip and (symmetric\$3 near3 (layout or architecture))	USPAT; US-PGPUB;	2003/10/17 12:25
		()	EPO; JPO;	
			DERWENT;	
L			IBM_TDB	

	.,		1	
-	307915	(processor same (PLL and cache)) and chip symmetric\$3	USPAT;	2003/10/17 12:26
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	107	processor near3 (logical adj unit)	USPAT;	2003/10/17 12:27
			US-PGPUB;	
			EPO; JPO;	†
			DERWENT;	
			IBM_TDB	
-	0	(processor near3 (logical adj unit)) same symmetric\$3	USPAT;	2003/10/17 12:42
			US-PGPUB;	·
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	1418	((processor or CPU) near3 (architecture or layout)) and	USPAT;	2003/10/17 12:43
İ		symmetric\$3	US-PGPUB;	
			EPO; JPO;	
			DERWENT:	
			IBM_TDB	
-	2	6176893.pn.	USPAT;	2003/10/17 12:44
			US-PGPUB;	
			EPO; JPO;	
			DERWENT:	
			IBM_TDB	
-	15	processor with (bump near3 array)	USPAT;	2003/10/17 14:18
		, , , , , , , , , , , , , , , , , , , ,	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
•			IBM_TDB	
-	0	(processor same (bump near3 array)) and (mask adj pattern)	USPAT;	2003/10/17 14:19
		(,,,,,,,,,	US-PGPUB;	
			EPO; JPO;	,
			DERWENT;	
			IBM_TDB	
_	1	(processor same (bump near3 array)) and mask	USPAT;	2003/10/17 14:50
		(4	US-PGPUB;	
		•	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
_	8337	processor same mask	USPAT;	2003/10/17 14:50
			US-PGPUB;	2000/10/17 11:00
		·	EPO; JPO;	
			DERWENT;	:
		·	IBM_TDB	
_	4738	processor with mask	USPAT;	2003/10/17 14:51
		· · · · · · · · · · · · · · · · · · ·	US-PGPUB;	
			EPO; JPO;	
			DERWENT:	
			IBM TDB	
-	261	processor with (mask near3 pattern)	USPAT;	2003/10/17 14:55
		,	US-PGPUB;	
	!		EPO; JPO;	
			DERWENT;	
			IBM TDB	
-	0	(each adj processor) with (mask near3 pattern)	USPAT;	2003/10/17 15:26
		, , , , , , , , , , , , , , , , , , , ,	US-PGPUB;	
			EPO; JPO;	
]			DERWENT;	
			IBM_TDB	
_	0	(each adj (processor or chip or IC)) with (mask near3 pattern)	USPAT;	2003/10/17 14:52
		The state of the s	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
]			IBM_TDB	;
	·			<u> </u>

-	0	(each adj (processor or chip or IC)) with mask	USPAT;	2003/10/17 14:52
1			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	1	(each adj (processor or chip or IC)) with pattern	USPAT;	2003/10/17 14:52
			US-PGPUB;	
			EPO; JPO;	·
			DERWENT;	
			IBM_TDB	
-	155	processor with (mask adj pattern)	USPAT;	2003/10/17 14:55
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	49	processor near3 (mask adj pattern)	USPAT;	2003/10/17 14:56
	,,,	processor real of critical and particularly	US-PGPUB;	2000/10/17 11:00
			EPO; JPO;	
			DERWENT;	•
			IBM_TDB	
1_	464	(processor or chip or IC) near3 (mask adj pattern)	USPAT;	2003/10/17 15:24
_	104	(mask auj pattern)	US-PGPUB;	2003/10/17 13.24
1			EPO; JPO; DERWENT;	
			1	
	0	mask adj pattern adj for adj processor	IBM_TDB USPAT;	2002/10/47 45:05
-	U	mask adj pattern adj for adj processor		2003/10/17 15:25
	ı		US-PGPUB;	
			EPO; JPO;	,
			DERWENT;	,
			IBM_TDB	
-	0	(each adj processor) same (mask near3 pattern)	USPAT;	2003/10/17 15:26
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	_		IBM_TDB	
-	0	(each adj processor) same mask	USPAT;	2003/10/17 15:42
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	:
			IBM_TDB	·
-	0	("each" adj processor) same mask	USPAT;	2003/10/17 15:42
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	44	processor same (mask adj "2")	USPAT;	2003/10/18 10:18
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	;
-	0	mask adj pattern adj for adj (processor or IC or semiconductor	USPAT;	2003/10/18 10:20
		or chip or device or (integrated adj circuit))	US-PGPUB;	
		, , , , , , , , , , , , , , , , , , , ,	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	2943	(mask adj pattern) near3 (processor or IC or semiconductor or	USPAT;	2003/10/18 10:20
		chip or device or (integrated adj circuit))	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	379	(mask adj pattern) near3 (processor or IC or semiconductor or	USPAT;	2003/10/18 10:21
		chip or device or (integrated adj circuit)) and ((mask adj	US-PGPUB;	
		pattern) near3 second)	EPO; JPO;	
		F=/,=/	DERWENT;	
			IBM_TDB	
L	L	L	100	L

-	270	(mask adj pattern) near3 (processor or IC or semiconductor or chip or device or (integrated adj circuit)) and ((mask adj	USPAT; US-PGPUB;	2003/10/18 10:22
		pattern) near3 second) and manufactur\$3	EPO; JPO; DERWENT;	:
			IBM_TDB	
-	57	(mask adj pattern) near3 (processor or IC or semiconductor or	USPAT;	2003/10/18 11:16
		chip or device or (integrated adj circuit)) and ((mask adj	US-PGPUB;	
		pattern) near3 second) and manufactur\$3 and (pattern near3	EPO; JPO;	
		(wiring or connect\$3 or intercoinnect\$3))	DERWENT;	
-			IBM_TDB	
-	0	processor same (p-MOS and n-MOS and gate near3 (source	USPAT;	2003/10/18 11:18
		and drain))	US-PGPUB; EPO; JPO;	
			DERWENT;	
			IBM TDB	
_	3	processor same (p-MOS and n-MOS and gate)	USPAT;	2003/10/18 11:26
		Freezest came (Final came came gand)	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	1		IBM_TDB	
-	0	(processor near3 (contain\$3 or hold43 or includ43)) near3	USPAT;	2003/10/18 11:29
		(p-MOS and n-MOS and gate)	US-PGPUB;	
			EPO; JPO; DERWENT;	
+			IBM TDB	;
-	0	processor near3 (p-MOS and n-MOS and gate)	USPAT;	2003/10/18 11:28
		, pro	US-PGPUB;	
	İ		EPO; JPO;	
			DERWENT;	
			IBM_TDB	0000404040
-	4371	processor near3 (transistor or p-MOS or n-MOS or gate)	USPAT;	2003/10/18 11:29
			US-PGPUB; EPO; JPO;	"
			DERWENT;	
			IBM TDB	
-	56	(processor near3 (contain\$3 or hold43 or includ43)) near3	USPAT;	2003/10/18 11:30
		(transistor or p-MOS or n-MOS or gate)	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	0	(processor poor? (contain\$2 or hold42 or includ42\) poor?	IBM_TDB USPAT;	2003/10/18 11:39
-		(processor near3 (contain\$3 or hold43 or includ43)) near3 (transistor or p-MOS or n-MOS or gate) and 716/\$.ccls.	US-PGPUB;	2003/10/10 11.39
		(transistor or p-weed or n-weed or gate) and 7 torp.cois.	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	(processor near3 (contain\$3 or hold43 or includ43)) near3	USPAT;	2003/10/18 11:39
		(transistor and gate)	US-PGPUB;	
			EPO; JPO;	
			DERWENT; IBM_TDB	
-	0	(processor near3 (contain\$3 or hold43 or includ43)) near3	USPAT;	2003/10/18 11:39
		(MOS and gate)	US-PGPUB;	
			EPO; JPO;	
	1		DERWENT;	
		//nunnannannannannannannannannannannannann	IBM_TDB	0000140140 44:40
	0	((processor or multiprocessor) near3 (contain\$3 or hold43 or includ43)) near3 (MOS and gate)	USPAT; US-PGPUB;	2003/10/18 11:42
		includas)) ricals (MOS and gate)	EPO; JPO;	
			DERWENT;	
			IBM_TDB	:
-	0	((processor or multiprocessor or microprocessor) near3	USPAT;	2003/10/18 11:42
		(contain\$3 or hold43 or includ43)) near3 (MOS and gate)	US-PGPUB;	
			EPO; JPO;	
			DERWENT; IBM_TDB	
l	L		מטו_ואוטו	

-	0	((processor or multiprocessor or microprocessor) near3	USPAT;	2003/10/18 11:42
		(contain\$3 or hold43 or includ\$3 or hav\$3 or has)) near3	US-PGPUB;	
		(MOS and gate)	EPO; JPO;	
			DERWENT;	
			IBM_TDB	ļ
-	0	((processor or multiprocessor or microprocessor) near3	USPAT;	2003/10/18 11:43
		(contain\$3 or hold\$3 or includ\$3 or hav\$3 or has)) near3	US-PGPUB;	
		(MOS and gate)	EPO; JPO;	
			DERWENT;	
			IBM_TDB	:
_	7	((processor or multiprocessor or microprocessor) near3	USPAT;	2003/10/18 15:16
		(contain\$3 or hold\$3 or includ\$3 or hav\$3 or has)) near3	US-PGPUB;	
		((MOS or transistor) and gate)	EPO; JPO;	
			DERWENT;	
			IBM_TDB	